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THESIS

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ABSTRACT

MOS technology and switched-capacitor design techniques have made it feasible to fully integrate active filters. The direct replacement of elements in passive RLC ladder structures with their bilinear equivalents is one method of realizing filters which retain the low sensitivity properties of passive RLC ladder filters. In this thesis a bilinear grounded inductor, which requires only one operational amplifier (op-amp) in its construction, is synthesized from a leap-frog parallel LC structure. In addition, several limits on and aspects of the performance of the bilinear inductor are covered. First, capacitor ratios and their errors as well as parasitic capacitance problems are analyzed and design considerations given that will improve the circuit's response. The influence of noise and nonideal op-amp characteristics on the dynamic range is also calculated and design improvements suggested. Op-amp gain and bandwidth effects are evaluated in terms of the inverting and noninverting integrators in the circuit, and it is determined that they have a negligible effect. Sensitivities, in relation to capacitor ratios, of a second-order, high-pass bilinear filter are calculated to show their similarities to passive RLC circuit sensitivities. Finally, a simple filter is simulated to verify its response and, by implication the bilinear grounded inductor's performance.

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CHAPTER I

INTRODUCTION

Prior to approximately 1970, high-quality analog filters were realized by meticulously selecting the capacitors, resistors and inductors used in passive RLC circuits. When the late 1960's saw the development of integrated-circuit operational amplifiers, emphasis shifted to realization and synthesis of active-network inductorless filters, otherwise known as active-RC circuits. Operational amplifiers allowed the designer to have control over the pole-zero locations of RC networks; thus, complex functions could be realized without the lossy characteristics, nonlinearities, bulk or noise generating features of real inductors. Unfortunately, complete integration of these active-RC filters is limited by the size of the resistors in the circuit. A single integrated resistor can take up as much as 10% of the area of a chip [3]. In addition, integrated resistors can have errors of ± 50% in their values. These errors are due to process variations, making active-RC filters impractical to integrate.

In the late 1970's, MOS technology made it possible to fully integrate active-RC and simulated RLC filters by converting these circuits to switched-capacitor configurations. MOS technology is preferred over bipolar technology for integrating filters because it has low-leakage charge storage, offset-free switches and non-destructive charge sensing [3]. As a result of these technological advantages, the technique of simulating a resistor by switching a capacitor between two MOS transistors became feasible. This simple concept is the basis of a multitude of

circuit designs known as switched-capacitor circuits, and it allows the integration of circuits that could not previously be fabricated.

In creating filters, active-RC circuits that realize first- and second-order transfer functions are routinely cascaded together to yield higher-order functions. Many active-RC structures have high-Q poles that are sensitive to component variations. This makes them unacceptable for integration due to tolerances in fabrication. Of primary interest, then, is the direct substitution of elements in a ladder structure which can be used to realize high-Q poles and has the added advantage of low sensitivities to component variations. The main focus of this thesis is the synthesis of one of these components, the inductor. More specifically, the development of a grounded, bilinear inductor for use in a high-pass, ladder structure filter.

Numerous papers have been written [6][7][10] on theoretical ways to simulate inductors; gyrators, general impedance converters and immittance converters are but a few of the approaches reported. Most of these methods realize floating inductors, but there are a few circuits [7][9] that model the grounded (shunt) inductors required in high-pass filters. Of these models, some [7] are based on the forward-Euler or backward-Euler z-transforms that, unlike the bilinear transform, induce distortion errors due to the transform's poor correlation between continuous-time and discrete-time signals. Most of these shunt inductor models also violate integrating design rules. The main rule violated is "The noninverting op-amp input should be kept at a constant voltage" [3]. Only a few circuits are known that use the bilinear transform and do not violate major design rules [9]. Another circuit selection criteria, which will help in

minimizing the circuit's size, is that the synthesized circuit should be constructed with only one op-amp.

Working within these limits, a circuit proposed by Burton [4] and further developed by Inoue and Ueno [8][9] can be used to create a bilinear, grounded inductor. The circuit is theoretical, and its development is vague from a mathematical standpoint. Also, these papers do not cover design limitations for integration nor limitations due to nonideal conditions. While the circuit does realize the inductor using only one op-amp, further development of this circuit is still needed and is the basis of this thesis.

OBJECTIVE

The original papers [4][8][9], which are wholly theoretical, that lead to and present the basic circuit for simulating a bilinear grounded inductor are unclear as to how the circuit was derived from an ideal, passive inductor, nor do the papers cover any of the practical aspects of integration or performance. Thus, the core of this thesis is the derivation of the governing equations for an inductor in both the s- an z domains and the development of the original circuit by Burton [4] into the bilinear grounded inductor of Inoue & Ueno [9]. Since none of these authors developed the circuit beyond theory, a chapter is devoted to addressing the limitations on the design due to integration requirements and basic nonideal effects. Finally, an application filter circuit is proposed and a computer simulation run to validate the circuit's use as a filtering component.

CHAPTER II

SYNTHESIS AND ANALYSIS

To synthesize the bilinear inductor of this thesis, it is expedient to first derive the Laplace and z-transform equations that describe an ideal inductor's impedance. Once known, these equations can be realized by ether a continuous-time or a sampled-data (switched-capacitor) circuit. Figure 2.1 depicts the voltage and current references for an ideal inductor. The differential equation describing this

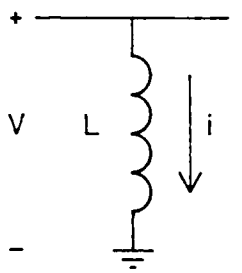

Figure 2.1. Ideal inductor.

relationship is

$$v(t) = L \frac{di(t)}{dt} \tag{2.1}$$

In the s-domain, equation (2.1) becomes

$$V(s) = sLI(s) \ ,$$

where the initial conditions are assumed to be zero. Impedance in the s-domain for an ideal inductor can now be defined by

$$Z(s) = \frac{V(s)}{I(s)} = sL \ . \tag{2.2}$$

For switched-capacitor circuits, charge transfer is of more interest than current. Therefore, using the current to charge relationship

$$i(t) = \frac{dq(t)}{dt} \quad ,$$

equation (2.1) becomes

$$v(t) = L \frac{d^2q(t)}{dt^2} \quad ,$$

and its s-domain equivalent is

$$V(s) = s^2LQ(s), \tag{2.3}$$

where the initial conditions again are zero.

Generally, switched-capacitor circuits are described in the z domain. Thus, equation (2.3) requires a s-to-z frequency transformation that approximates its continuous-time properties.

There are several methods for converting s-plane equations to the z domain: forward Euler, backward Euler and bilinear transformations. Of all the simple frequency transforms, only the lossless discrete integrator (LDI) and the bilinear transformations map the imaginary axis in the s-plane to the unit circle in the z-plane. This property is necessary if the discrete time transfer function's loss response, except for frequency warping effects, is to be the same as the continuous-time loss response [12]. Usually, the LDI transform method is preferred since the derived circuits can normally be made insensitive to parasitic capacitances [12]. Unfortunately, resistive terminations for LDI type ladder filters can not

be realized directly and can only be approximated. Briefly, in frequency transformations a difference operation replaces continuous-time derivatives, but the sampling points used for the LDI transform difference approximation are not the same as for the original function [12]. As a result, the LDI transformation of ladder network terminations can only be approximated. These approximations cause the frequency response to deviate substantially from the desired response. Unlike the LDI transform, the bilinear transformation's sampling points are the same points used for a continuous-time derivative; consequently, exact terminations can be realized. Therefore, the bilinear s-to-z frequency transformation will be utilized and is defined by

$$s = \frac{2}{T}\,\frac{1 - z^{-1}}{1 + z^{-1}} \quad .$$

Before equation (2.3) can be converted to a discrete time function, a few other notational clarifications are needed. First, V(s) becomes $V^e(z)$ and Q(s) becomes $Q^e(z)$ to indicate sampled values; superscripts indicate that the quantities represent the total voltage and charge at the end of the even phase. In addition, a differential charge $\Delta Q^e(z)$ must be explained and defined. $\Delta Q^e(z)$ is the discrete time equivalent of current, usually described by a difference equation. It can also be thought of as the difference between the total charge at the end of the n^{th} even phase and the total charge at the end of the $(n-1)^{th}$ even phase, or if no variation in charge occurs during the odd phase, the total charge at the beginning of the n^{th} even phase. The z domain representation of the difference equation is [11]:

$$\Delta Q^e(z) = Q^e(z)(1 - z^{-1}). \qquad (2.4)$$

Finally, returning to equation (2.3) and making all the appropriate substitutions, the discrete time admittance becomes

$$\frac{\Delta Q^e(z)}{V^e(z)} = \frac{T^2}{4L} \cdot \frac{(1 + z^{-1})^2}{(1 - z^{-1})} \quad , \qquad (2.5)$$

which models a bilinear inductor in the z domain.

Having derived the defining equations, the next step is to find a continuous-time circuit that realizes equation (2.2). Then, convert this circuit to an equivalent switched-capacitor configuration that yields the bilinear inductor of equation (2.5).

Knowing before hand where the analysis will lead, a portion of a leap-frog circuit, proposed by Burton [4] and expanded by Inoue & Ueno [8][9], will first be examined. Illustrated in figure 2.2, this circuit simulates a grounded parallel LC structure.

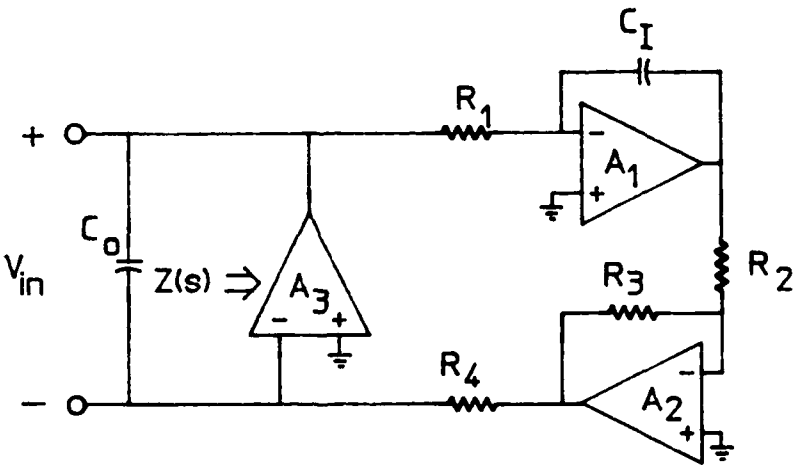

Figure 2.2. Parallel LC simulation circuit.

An analysis of figure 2.2, based on ideal elements, is as follows;

$$I_{in} = I_{out} \quad , \quad I_{out} = \frac{V_2}{R_4}$$

$$V_2 = \frac{-V_1 R_3}{R_2}, \qquad V_1 = \frac{-V_{in}}{sC_I R_1}$$

Making substitutions and solving for the impedance gives

$$Z(s) = \frac{V_{in}}{I_{in}} = \frac{sC_I R_1 R_2 R_4}{R_3}$$

which is essentially the same as equation (2.2). A large range of inductance can be achieved with this configuration; since, for equal R, the equivalent inductance is determined by $C_I R^2$. The feedback capacitor C_o is required in the circuit for the analysis to be valid, so the circuit can only simulate a parallel LC structure. Surprisingly, when modified, this circuit's switched-capacitor equivalent circuit realizes a grounded bilinear inductor.

In converting the configuration of figure 2.2 to a switched-capacitor circuit, two of three changes are easily made. First, R_1 is replaced by a parallel switched-capacitor realization with C_L as the switched element. Next R_2, R_3 and A_2 act as an inverter, but their inverting effect can be achieved by replacing R_4 with an inverting switched capacitor, C_f (see figure 2.3), making it possible to completely remove R_2, R_3 and A_2. Finally, for the third change, the op-amp A_3 should be removed. The result would then be a one op-amp, simulated inductor which would be highly desirable for exact element replacement in ladder networks.

It is not intuitively obvious how A_3's removal can be accomplished. Inoue & Ueno [2] propose what is basically a phase sharing of the single op-amp A_1. In other words, it can be shown that op-amp A_1 does not have

any redistribution of charge associate with it during the even phase if op-amp A_3 remains and the same is true for A_3 in the odd phase. Therefore, the function of A_1 and A_3 can be accomplished with a single op-amp when elements are properly switched. The end result of all these conversions is given in figure 2.3 where the squares represent the ideal switches, and the labels indicate the phase, even or odd, when the switches are closed. Figure 2.3's circuit can also be constructed by using Ineuo & Ueno's [10] switched-capacitor immittance converter which gives the same results.

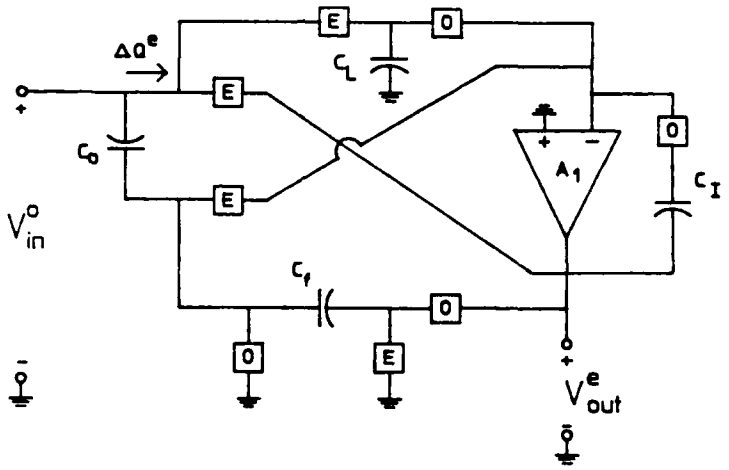

Figure 2.3. Switched-capacitor simulated inductor.

To analyze this circuit using the method of charge conservation, it is best to look at the equivalent circuits for each phase. In figures 2.4 & 2.5 the even and odd phase equivalent circuits are shown where the superscripts denote even and odd phase voltages. $V_{in}^e(n)$ is the even phase output voltage of the op-amp. During the odd phase, $V_{in}^o(n)$ is the input voltage only on the capacitor C_o.

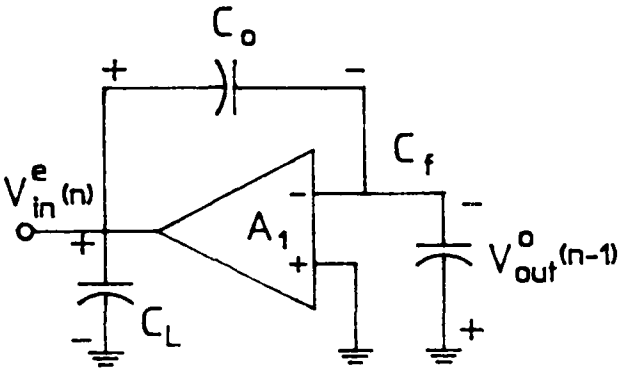

Figure 2.4 Even phase equivalent circuit.

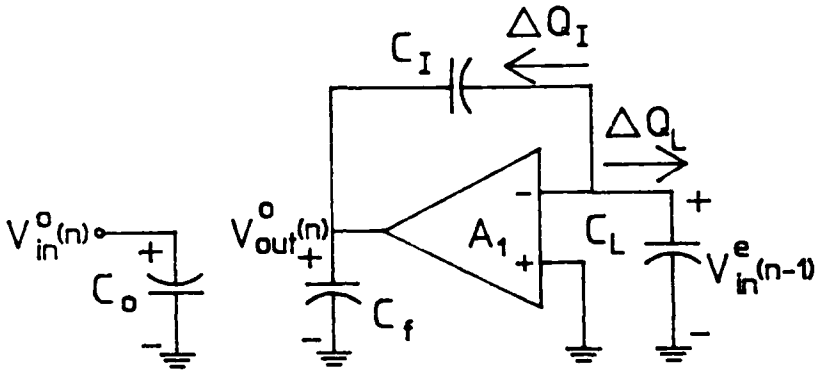

Figure 2.5 Odd phase equivalent circuit.

A differential charge, $\Delta Q^e(n)$, during the even phase is equivalent to the change in charge on capacitors C_L and C_o at the end of the even phase. Mathematically, it is stated as

$$\Delta Q^e(n) = C_L V^e_{in}(n) + C_o[V^e_{in}(n) - V^o_{in}(n-1)] \ .$$

During the odd phase, the change in charge at the input is

$$\Delta Q^o(n) = C_o V^o_{in}(n) - C_o V^e_{in}(n-1)$$

where n-1 indicates the input voltage during the previous period for the

superscripted phase. The differential charge for the even phase is written as

$$\Delta Q^{e}(n) = C_L V_{in}^{e}(n) + C_o[V_{in}^{e}(n) - V_{in}^{e}(n-1)] ,$$

and is also equal to

$$\Delta Q^{e}(n) = -C_f V_{out}^{o}(n) \tag{2.6}$$

A transfer function relating $V_{out}^{o}(n)$ to $V_{in}^{e}(n-1)$ is determined as follows;

$$\Delta Q_L^{e} = C_L V_{in}(n-1),$$

$$\Delta Q_I = -C_I[V_{out}^{o}(n) - V_{out}^{o}(n-1)] ,$$

where ΔQ's subscripts indicate the change in charge on the subscripted capacitor. It can be seen in figure 2.5 that

$$\Delta Q_I = \Delta Q_L .$$

Hence,

$$-C_I[V_{out}^{o}(n)-V_{out}^{o}(n-1)] = C_L V_{in}^{e}(n-1) .$$

After applying the z-transform, the solution for $V_{out}^{o}(z)$ is

$$V_{out}^{o}(z) = \frac{-z^{-1}C_L}{C_I(1 - z^{-1})} V_{in}^{e}(z) . \tag{2.7}$$

Substituting equation (2.7) into equation (2.6) gives

$$\Delta Q^e(z) = -\frac{C_f C_L}{C_I} \frac{z^{-1}}{1 - z^{-1}} V_{in}^e(z) \ . \qquad (2.8)$$

Equation (2.8) specifies a LDI type inductor admittance. Using equation (2.4) and the algebraic relation proposed by Lee [11], namely

$$\frac{z^{-1}}{(1 - z^{-1})^2} = \frac{1}{4} \frac{(1 + z^{-1})^2}{(1 - z^{-1})^2} - \frac{1}{4} \ ,$$

equation (2.8) becomes

$$\frac{\Delta Q^e(z)}{V_{in}^e(z)} = \frac{T^2}{4} \cdot \frac{(1 + z^{-1})^2 C_f C_L}{(1 - z^{-1}) C_I T^2} - \frac{C_f C_L (1 - z^{-1})}{4 C_I} \ , \qquad (2.9)$$

which represents a bilinear inductor in parallel with a negative capacitor. It is interesting to note that the capacitor, C_o, is not part of the final equation. The reason is that equation 2.9 is only the admittance of the circuit looking to the right of the capacitor, C_o. This circuit is still a parallel LC circuit but now C_o can be used to cancel the negative capacitance if it is set equal to $C_f C_L / 4C_I$. The circuit in figure 2.3 can then simulate a bilinear grounded inductor or, if needed, a parallel LC structure.

The equivalent inductance is defined as

$$L_{eq} = \frac{T^2 C_I}{C_f C_L} \ .$$

Theoretically, a large range of inductance can be realized by this circuit even when the circuit is used in a high-pass ladder network (ie T is small for high-pass filters).

Unfortunately, there are bounds on what this circuit can achieve as an integrated circuit due to nonideal conditions. The following chapter will cover limitations and nonideal effects related to the proposed circuit.

CHAPTER III

3.1 INTRODUCTION

Theoretically the bilinear inductor derived in chapter II satisfies the requirements for a grounded inductor that can be used in a high-pass ladder structure filter. However, nonideal conditions effect the actual performance of circuits, especially when the filter is to be integrated. The following sections explore design restrictions and nonideal aspects that apply directly to the proposed circuit. While other topics, such as clock feedthrough and antialiasing circuits, are relevant to switched-capacitor circuit design, they are beyond the scope of this thesis and will only be discussed when and where they have an influence on the circuit.

3.2 CAPACITOR RATIOS

As mentioned in the introduction, switched-capacitor techniques make it possible to fully integrate filters. In order for such a filter to be accurately realized using switched-capacitor filtering techniques, the filter's transfer function must be a function of capacitor ratios instead of the absolute value of a capacitor. It is an established fact [2] that random process variations can change the absolute value of an integrated capacitor by as much as 10-20 percent. In contrast, special processing and proper layout techniques have made it possible to realize monolithic MOS capacitor ratios to an accuracy of 0.1 percent [2]. Hence, the dependence on ratios to realize functions.

It can be assumed that any attempt to integrate the proposed theoretical circuit would involve choosing a fabrication process and design geometries that will minimize ratio-matching errors. While selecting a process or geometry is beyond the scope of this thesis, a few common design practices can be used to reduce ratio-matching errors and allow the ratio accuracy figure of 0.1% to be used. One such procedure is the use of common unit-capacitor layouts to reduce systematic errors. For example, one capacitor in a ratio would be a unit-capacitor, while the other would be made of an array of unit-capacitors, plus a single odd shaped capacitor. More accuracy is possible if the capacitor ratio can be implemented with integer multiples of the unit-capacitor. Another error affecting ratios is associated with the periphery-to-area ratio of one capacitor in relation to the other capacitor [1]. Basically, the periphery-to-area ratio for both capacitors in a ratio should be identical to reduce process error effects. The periphery-to-area ratio accuracy decreases as the ratio of the two capacitors deviates from 1:1 and is more severe as the absolute value of the capacitance gets smaller. With these procedures in mind, the two critical ratio relationships in the theoretical circuit can be evaluated.

If the circuit is to simulate a bilinear inductor, a capacitor, C_o, must be scaled to cancel the negative capacitor defined by $-C_f C_L/4C_I$. Since the capacitors C_L and C_I are related to each other in the integrating portion of the circuit, the ratios should be designated as

$$\frac{C_o}{C_f} = \frac{C_L}{4C_I} \quad . \tag{3.1}$$

Fortunately, this designation allows the error due to capacitor ratio deviation to be minimized and keeps the capacitor values as integer multiples of the unit capacitance if the ratios are chosen as

$$\frac{C_o}{C_f} = \frac{1}{2} \quad , \quad \frac{C_L}{C_I} = 2 \quad , \tag{3.2}$$

which gives 2:1 ratios with C_o and C_I as unit-capacitors. Whether a given capacitor is actually a set of unit-capacitors depends on the values needed to realize ω_o and Q of the filter, but equation (3.2) does show how close the ratios can be kept.

Equation (3.1) will not be exact due to ratio errors. Since the ratios are defined in accordance with standard methods, the 0.1 percent error figure for ratios is acceptable for determining accuracy. A worse case cancellation error for the two ratios can be determined as follows:

$$\Delta e = \frac{C_o}{C_f}(1 \pm 0.001) - \frac{C_L}{4C_I}(1 \pm 0.001) \ ,$$

which, when normalized and solved, gives

$$e_n = (1 \pm 0.001) - (1 \pm 0.001) = 0.002 \ .$$

Thus, the maximum error in cancelation is 0.2 percent.

An additional problem is that the MOS switches are not ideal, and some charge injection is possible through them from the clocking circuitry [5], which will distort the response. To overcome this adverse effect the integrating capacitors C_I and C_o should be made as large as practical. For C_o, this requirement contradicts the need for C_o to be equal to a small negative capacitance.

Another critical ratio is found in the definition for the bilinear inductance which is defined as

$$L = \frac{T^2 C_I}{C_f C_L} \quad ,$$

where T is the sampling period. Based on the previously stated conditions for ratios, the inductance can be restated as

$$L = \frac{\alpha\, T^2}{C_f} \quad ,$$

where α is a constant equal to the capacitor ratio C_I/C_L.

For the bilinear transform assumption to remain valid, the clock frequency, $f_c = 1/T$, must be much greater than the highest frequency in the sampled signal [5]. More importantly, this clock frequency is determined by a quartz-crystal-controlled clock circuit which is very accurate and stable [5]. As a result, the inductance can be said to be inversely proportional to the absolute value of the capacitor C_f. Hence, for a fixed clock frequency, the inductance will inherit the same 10-20 percent error that integrated capacitors have.

Controlling the inductance by adjusting the clock period is possible. It is known that the variation in the absolute value of monolithic capacitors across a wafer is primarily due to changes in the dielectric thickness; however, the matching of two identical capacitors within the same die area has an accuracy of 0.1 ⇒ 1.0 percent [5]. Since the errors effect each capacitor on the chip in the same way, each shunt inductor's value will have the same percentage error as all the other shunt branches.

This makes it possible to adjusted each of their values at the same time by changing the clock period T.

Realizing a specified inductance is not possible given the poor control over the absolute value of a capacitor, but controlling the inductance by changing the clock frequency is possible. It will be shown in the section on sensitivity that, in the second order example filter, ω_o and Q are functions of controllable capacitor ratios, adding more accuracy to realizing filter functions. Generally, when the inductor is used in a filter configuration, the poles are set as a function of LC. Since the inductance was defined as being inversely proportional to a capacitor, the poles are now defined as functions of capacitor ratios and not the absolute value of the inductor, L.

3.3 *PARASITIC CAPACITANCE*

The process of integrating switched-capacitor circuits introduces unavoidable parasitic capacitances that could, if not minimized or eliminated, render the circuit useless or could significantly degrade the filter's response. Voltage gains in switched-capacitor filters depend only on the ratios of the circuit's capacitors [5], but those ratios can be distorted by parasitics. Of all the various stray capacitances, only those that effect the accuracy of these ratios are of interest. The simulated inductor of figure 2.4 is not a fully stray-insensitive circuit: hence, capacitor values are affected by the parasitics that are associated with the P-N junctions and the interconnecting leads of the MOS switches [5]. There are four different switching schemes for the capacitors used

in the simulated inductor circuit. Each of these schemes must be looked at separately to determine which parasitics are important.

First, the parallel switched capacitor C_L is considered. Shown in figure 3.1, C_L has all the pertinent parasitics identified.

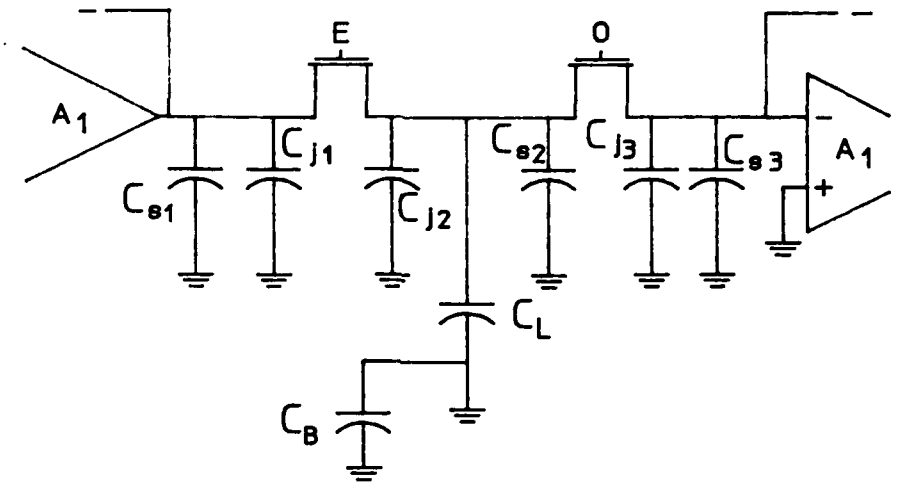

Figure 3.1 C_L's parasitic capacitances.

Interconnect capacitances are labeled as C_{si}, and the junction capacitances as C_{ji}. The bottom plate to substrate capacitance is denoted as C_B. For the parallel switched capacitor C_L, parasitics C_{s1} and C_{j1} are driven by a low impedance source so they can not add charge to C_L. The same is true for C_{s3} and C_{j3} since they are at the virtual ground of the op-amp. Since the bottom plate of C_L is grounded, C_B's effects can be ignored as well. Thus, C_{s2} and C_{j2} are the only critical parasitics. Since they are in parallel with C_L, they increase the effective value of C_L by increasing the amount of charge transferred when C_L is switched. Unless C_{s2} and C_{j2} are kept small, and C_L made large to swamp out the effects of these parasitics, their influence can significantly distort the effective ratio C_I/C_L, which partially determines the simulated inductor's

value. Besides making C_L as large as possible, C_L could be made slightly smaller than the design requires to compensate for the added parasitic capacitances. Another justification for swamping out the parasitics by increasing C_L is that the junction capacitance C_{j2}, which is voltage dependent, adds a nonlinear effect to the effective capacitance ratio that would be minimized by C_L's increase.

The inverting switched capacitor C_f is the second capacitor to be examined. Figure 3.2 shows C_f and its associated parasitics. Arguments for C_{j1}, C_{s1}, C_{j3} and C_{s3} given for C_L in figure 3.1 hold for C_f in figure 3.2, and since the junction capacitances C_{j4} and C_{j5} are grounded out, they can be ignored as well.

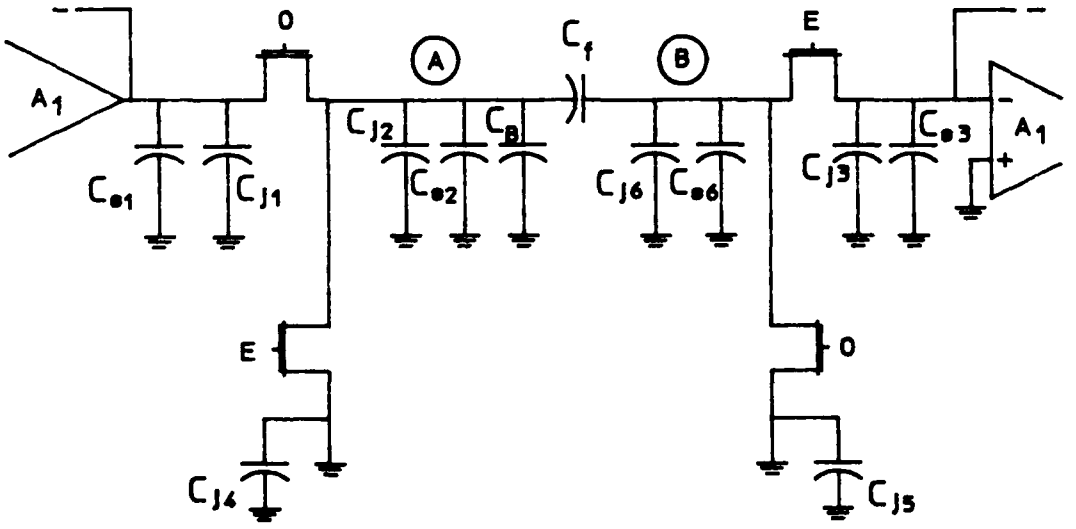

Figure 3.2 Inverting capacitor C_f.

Nodes A and B are the important stray capacitance points. The parasitics at point A are periodically charged from a low impedance source, and are then discharged to ground which leaves C_f unaffected. Point B's parasitics are grounded for both halves of the period; one ground is

through a switch and the other is a virtual ground. Note that the bottom plate of C_f is connected to the output of the op-amp. This is done because the bottom plate parasitic capacitance can be as much as 5%-20% of C_f while the top plate is only 0.1% to 1% [5]. Driving the bottom plate with a low impedance source eliminates problems with the large bottom plate parasitic. The smaller top plate parasitic is at the virtual ground of the op-amp which minimizes error. While the virtual ground assumption is usually implied in ideal cases, it is valid for this discussion as long as the unity-gain bandwidth frequency of the op-amp is at least five times as large as the clock frequency [5]. This gives the circuit sufficient settling time so that any charge accumulated on the parasitics at the inverting input of the op-amp during a given phase will have time to be redistributed back into the circuit by the end of the same phase. Thus, the error is negligibly if these design constraints are heeded.

The integrating capacitor, C_I, is the third switched capacitor to be analyzed. C_I's parasitics are given in figure 3.3.

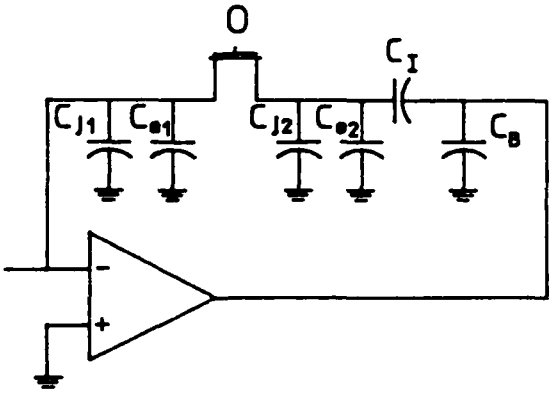

Figure 3.3 Integrating capacitor parasitics.

C_I's top plate is periodically switched to a virtual ground which renders the junction and interconnect capacitances harmless when the

previously noted frequency restraint is obeyed. A low impedance source drives the bottom plate of C_I so the bottom plate to substrate capacitance, C_B, can be ignored as well. C_I's top plate is switched out of the circuit during each even phase. When this happens the MOS transistor switch connected to C_I is off and a reverse biased P-N junction exists at the top plate. The leakage current, I_L, through this junction is small but can significantly discharge C_I if the switching period is too long. It is known that at room temperature the leakage current density, J_L, is approximately 1.55×10^{-14} A/um^2. This leakage density doubles for every 10°C rise in temperature [5]; for calculation purposes this correction, K_T, can be determined by

$$K_T = 2^{\left[\frac{T_{actual} - T_{room}}{10^{o}c}\right]}$$

The junction area is another factor in determining the leakage current. Assuming the use of minimum sized transistors as switches, the contact area is about 36μm^2 for a MOSIS 3μm CMOS process. For the maximum commercial temperature limit of 70°C, the leakage current can be determined as

$$I_L = (1.55 \times 10^{-14}\ A/\mu m^2) \times 2^{((70° - 25°)/10°))} \times 36\mu m^2$$

$$= 1.2626 \times 10^{-11}\ A$$

Of primary interest is the voltage loss from the capacitor with respect to time which can be determined by

$$\frac{dv}{dt} = \frac{I_L}{C} .$$

For a worse case estimate, a minimum sized integrated capacitor of 0.5pf is used. Thus,

$$\frac{dv}{dt} = 25.252 \text{ v/sec} .$$

Hence, the reverse P-N junction loss is only a few millivolts or less for switching frequencies above 10khz. The capacitor that actually has this loss is a large integrating capacitor C_I. This factor, and the circuit's intended use in a high-pass filter, which requires high frequency sampling, reduces the loss to a negligible level, eliminating the need for any design corrections.

The next capacitor to be analyzed is C_o which serves as a charge injecting capacitor during the odd phase, see figure 2.5, and as a integrating capacitor, exactly like C_I, during the even phase. When C_o acts as a integrating capacitor, the pervious argument for C_I applies except that there is no leakage charge when C_o is switched away from the op-amp. Instead, when C_o is switched to its odd phase position, its top plate is connected to ground, eliminating any parasitics. Its bottom plate is switched to an external voltage to allow for charge injection. The bottom plate parasitic will receive a charge at this point, but it will have no effect when C_o is switched back to its integrating capacitor position because it will be at the low impedance output of the op-amp.

It can be concluded that the circuit does have problems with parasitics. If C_L and C_I are kept as large as possible and the clock frequency kept to less than a fifth of the unity-gain bandwidth frequency of the op-amp, the circuit will realize the required impedance.

3.4 DYNAMIC RANGE

MOS operational amplifiers are the main active devices used to build switched-capacitor circuits. As a consequence, the op-amp's performance dominates many characteristics of the overall circuit, including the circuit's dynamic range. The MOS transistors that are used to build these op-amps and circuit switches limit the minimum input voltage threshold. The maximum input voltage is limited only by the op-amp's linear characteristics.

Dynamic range can be defined as the range of input signal amplitudes, from maximum to minimum, that the circuit can successfully process. The maximum voltage limit, $V_{in,max}$, is controlled by the linear range of the op-amp and can be described as the voltage input level for which the output signal has no significant nonlinear distortion. The minimum voltage limit is restricted by numerous spurious signals such as noise, clock feedthrough and low-level distortion [5]. Thus, $V_{in,min}$ is the smallest input signal that can be detected and used without notable interference. Using these two definitions of input signals, the dynamic range can be determined and is defined as

$$DR = 20 \log_{10} [V_{in,max} / V_{in,min}],$$

given in decibels.

An op-amp operating under open-loop conditions exhibits a dynamic range of only 30-40 dB [5]. Negative feedback configurations in the

simulated inductor circuit will produce a much larger range. To approximate the limits on the input values and the dynamic range for the simulated inductor, a noise model is required that incorporates the limiting noise signals.

Various noise sources contribute to the noise level that limits the minimum input signal amplitude. Each of these sources are made up of several types of noise: flicker noise, thermal noise and sample & hold noise. They are primarily associated with the MOS transistors and a sampling enigma. First, the flicker noise in MOS transistors comes from extra electron energy states in the boundary between the Si and SiO_2. These states can trap and release electrons from the channel, creating noise [5]. The process is slow so this noise source is only dominant for low frequency signals and can be ignored in this case since the simulated inductor will be part of a high-pass filter. Next, the thermal noise of the MOS transistors has a constant power spectral density, which means there is thermal noise present at all frequencies of interest. This thermal noise is associated with both the MOS transistors used as switches and those used in the op-amp. Finally, the sample and hold noise is caused by thermal noise being sampled and held on the input capacitor. This is a serious noise source problem because sampling causes aliasing of the noise spectrum, which will concentrate the noise power into the baseband. Sample & hold noise is directly proportional to the op-amp bandwidth, which can be controlled. The bandlimiting performed by the op-amp can reduce the amount of power aliased into the baseband; hence, ω_o of the op-amp should be as low as possible while still allowing enough settling time. As stated before, the op-amp's bandwidth frequency should

be five times the clock frequency [5] to allow for this required settling time. Three noise sources should be incorporated into the model to adequately represent the noise problems stated above. Each of these noise sources is a function of the sample & hold noise. $V_{n,1}$ is also a function of the op-amp's thermal noise, $V_{n,2}$ is a function of the thermal noise associated with the integrating capacitor's switch and $V_{n,3}$ is the thermal noise of the switch connected to the input capacitor, C_1, see figure 3.4. The noise analysis for both phases of the circuit can be accomplished in this manner because during each phase the noise model is exactly the same, only the capacitors change.

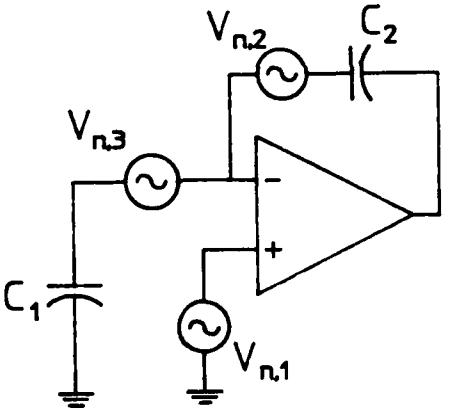

Figure 3.4 Noise model.

First, the voltage gain for each phase of the circuit, in the absence of noise, can be stated as

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{1}{A} + \frac{C_2}{C_1}\cdot\frac{(1+A)}{A}} , \qquad (3.3)$$

where A is the open-loop gain, C_2 is either C_I or C_o and C_1 is either C_L or C_f depending on the phase (see figures 2.3 & 2.4). The RMS output noise, $V_{o,noise}$, due to each of the three noise sources is defined as follows:

$$V_{o,noise1} = \frac{V_{n,1}}{\frac{1}{A} + \frac{C_2}{C_1 + C_2}} , \tag{3.4}$$

$$V_{o,noise2} = \frac{V_{n,2}}{1 + \frac{C_1 + C_2}{A\ C_2}} , \tag{3.5}$$

and

$$V_{o,noise3} = \frac{V_{n,3}}{\frac{1}{A} + \frac{C_2\ (1 + A)}{C_1 \quad A}} . \tag{3.6}$$

A minimum input signal, $V_{in,min}$, will induce an output signal approximately equal to the total output noise voltage, $V_{o,noise}$. Thus, with

$$V_{in,min} = V_{o,noise1,2,3}\left[\frac{1}{A} + \frac{C_2(1 + A)}{C_1 A}\right] , \tag{3.7}$$

and $A \gg 1$ for the frequencies of interest, equations 3.4-3.7 reduce to

$$V_{in,min} \simeq V_{n,1}\frac{C_1 + C_2}{C_1} + V_{n,2}\frac{C_2}{C_1} + V_{n,3} , \tag{3.8}$$

which defines the minimum input voltage in terms of the noise signals.

To determine the maximum input voltage, it is assumed that $V_{o,max} = V_{cc}$, the power supply voltage. Therefore,

$$V_{in,max} = V_{cc}\left[\frac{1}{A} + \frac{C_2}{C_1}\cdot\frac{(1 + A)}{A}\right] \simeq V_{cc}\frac{C_2}{C_1} \qquad (3.9)$$

Given the definition for the dynamic range and equations 3.8 & 3.9 the dynamic range can be approximated by

$$DR \simeq 20\log_{10}\left[\frac{V_{cc}}{V_{n,1}\frac{C_1 + C_2}{C_2} + V_{n,2} + V_{n,3}\frac{C_1}{C_2}}\right] . \qquad (3.10)$$

It is clear from equation 3.10 that reducing the noise voltage will significantly improve the dynamic range.

Several things can be done at the design level to limit the noise voltages. Bandlimiting by the op-amp, mentioned earlier, can be used to effectively reduce sample & hold noise. Increasing the size of the circuit's capacitors will increase the signal to noise ratio which reduces all noise effects [5]. Scaling of the capacitors for maximum dynamic range is another possibility, and reducing the incremental channel resistance of the MOS transistors will also reduce the noise voltage. Hence, any technique aimed at minimizing the noise will improve the dynamic range.

3.5 GAIN AND BANDWIDTH EFFECTS

Operational amplifiers used in active filters have finite dc gains, A_o, and bandwidthes, ω_t, that can greatly effect the magnitude and phase performance of continuous-time circuits. For the sampled-data circuit of this thesis, the effects of these nonideal characteristics on the impedance simulated by the circuit are of primary importance. Gain and bandwidth effects are usually calculated in relation to a voltage transfer function. While the simulated inductor is basically analyzed as an impedance, it can be separated into two types of integrators whose voltage transfer functions can be evaluated for nonideal op-amp effects.

To simplify the understanding of this analysis, the circuit is shown in figure 3.5 as two separate circuits, one for each clock phase; first as a inverting integrator during the odd clock phase figure 3.5(a), and as a noninverting integrator during the even clock phase, figure 3.5(b).

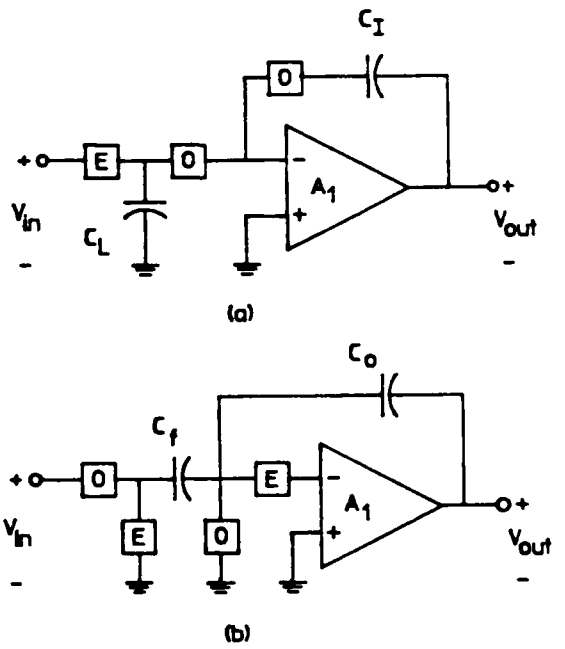

Figure 3.5 Integrators a) Inverting. b) Noninverting.

The following analysis is based on a paper by Martin and Sedra [13].

It can be shown that for an ideal op-amp the inverting integrator of figure 3.5(a) has a transfer function

$$H_i(e^{j\omega T}) = \frac{-C_L/C_I \; e^{\,j(\omega T/2)}}{j2 \sin(\omega T/2)} ,$$

and for the noninverting integrator of figure 3.5(b), the transfer function is

$$H_i(e^{j\omega T}) = \frac{C_f/C_o \; e^{\,-j(\omega T/2)}}{j2 \sin(\omega T/2)} ,$$

where $T = 1/f_c$ is the clock period and f_c is the clock frequency. It can also be shown that for small errors the actual transfer function can be expressed as

$$H_a(e^{j\omega T}) \simeq \frac{H_i(e^{j\omega T})}{1 - m(\omega) - j\theta(\omega)}$$

where $m(\omega)$ is the magnitude error and $\theta(\omega)$ is the phase error. For a finite dc gain, A_o, the actual transfer function for both integrators is

$$H_a(e^{j\omega T}) = \frac{H_i(e^{j\omega T})}{1 + \frac{1}{A_o}(1 + C_1/2C_2) - \frac{jC_1/C_2}{2A_o \tan(\omega T/2)}}$$

where C_1 is C_L and C_2 is C_I for the inverting integrator and C_1 is C_f and C_2 is C_o for the noninverting integrator. For $\omega_o T/2 \ll 1$, the errors in

magnitude and phase due to the finite dc gain can be given for both integrators as

$$m(\omega_o) \simeq -1/A_o \qquad \theta(\omega_o) \simeq 1/A_o \quad ,$$

where ω_o is the integrator unity-gain frequency. A_o is usually much much greater than 1, so the errors due to finite gain alone are negligible and equivalent to having capacitor ratio errors of the same magnitude.

To find the effects of the op-amp's finite bandwidth, the authors, Martin and Sedra [13], carried out a complex time-domain analysis based on a one pole amplifier gain model. The analysis is long, tedious and beyond the scope of this thesis; the reader is referred to the reference for details. The results of their work, however, are very useful in evaluating errors due to the finite unity-gain bandwidth, f_t. For $\omega_o T \ll 1$, the magnitude error for both integrators is

$$m(\omega_o) \simeq -2\pi(f_o/f_c)e^{-\pi f_t/f_c} \quad . \tag{3.7}$$

Since the requirement of $f_t > 5f_c$, which was chosen in the section on parasitic capacitance, still holds, the error will be small. The phase error for the noninverting integrator is zero, but the inverting integrator has a phase error approximately equal to the magnitude error of equation 3.7.

The independent nature of the two clock phases of the simulated inductor circuit allows the errors to be determined separately. The total

error is a summation of both clock phase errors. Since the errors in both phases are negligible, only minor effects should be expected from the finite characteristics of the op-amp. This is a common result for most switched-capacitor circuits because most designs allow enough time for settling between samples; consequently, there is little or no effect from nonideal op-amps.

3.6 SENSITIVITY

For active-RC circuits, sensitivity functions can be used to determine the effects of component variations and finite gain-bandwidth on the filter's performance. Switched-capacitor circuits can also be analyzed for sensitivity, although for some circuits the analysis is complex. Fortunately, as was demonstrated in the previous section, gain-bandwidth effects are negligible for the simulated inductor circuit and for most switched-capacitor circuits. This fact and the simulated inductor's intended use as a direct replacement for a passive inductor makes it easy to determine component sensitivities. Furthermore, ω_o and Q can be determined directly from the s-domain transfer function derived from the analog reference filter, ARF, given in figure 3.6.

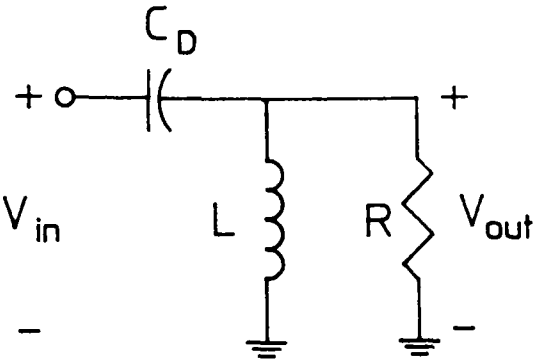

Figure 3.6 Analog reference filter.

A sensitivity function can be defined as the limit of a small relative change in one parameter divided by a small relative change in a second parameter as the second parameter's partial change approaches zero. This can be symbolized as

$$S_q^r = \lim_{\Delta q \to o} \frac{\frac{\Delta r}{|r|}}{\frac{\Delta q}{q}} = \frac{q}{|r|}\frac{\delta r}{\delta q}$$

where r is a function of q and q is the changing parameter.

Equation 3.8 can be derived from the high-pass ARF circuit of figure 3.6 and can be used to determine ω_o and Q. The s-domain voltage transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{s^2}{s^2 + s\frac{1}{C_D R} + \frac{1}{LC_D}} \qquad (3.8)$$

where C_D is the series capacitor of the second-order filter, R is the termination resistor, and L is the shunt inductor that is simulated by the proposed circuit. Since a ladder structure is used to allow the direct replacement of elements, L and R can be replaced by their bilinear equivalents. A bilinear resistor given by Lee [11] has an equivalent resistance of $T/2C_R$. After the elements are replaced, the transfer function becomes

$$\frac{V_{out}}{V_{in}} = \frac{s^2}{s^2 + s\frac{2C_R}{TC_D} + \frac{C_f C_L}{T^2 C_D C_I}}$$

where C_R is associated with the bilinear resistor and T is the clock period. Now ω_o and Q can be determined and are

$$\omega_o = \frac{1}{T}\sqrt{\frac{C_f C_L}{C_D C_I}} \quad , \qquad Q = \frac{C_D}{2C_R}\sqrt{\frac{C_f C_L}{C_D C_I}} \quad .$$

For switched-capacitor circuits, ω_o and Q are functions of capacitor ratios instead of absolute values. Thus, determining sensitivities with respect to each component does not provide much useful information but, sensitivities with respect to capacitor ratios does (one exception is the sensitivity to the clock period, T). Capacitor ratio errors can be controlled, so sensitivities related to these ratios are important. The component ratios of interest are

$$q_1 = C_L/C_I \quad , \quad q_2 = C_f/C_{D1} \quad , \quad q_3 = C_{D2}/C_R \quad .$$

C_{D1} and C_{D2} are the same capacitor, but it is defined in this manner to allow the sensitivities to be calculated for errors in ratios. Now ω_o and Q can be redefined as

$$\omega_o = \frac{1}{T}\sqrt{\frac{C_f C_L}{C_{D1} C_I}} \quad , \qquad Q = \frac{C_{D2}}{2C_R}\sqrt{\frac{C_f C_L}{C_{D1} C_I}} \quad .$$

It can be seen from the equation for Q that the ratios C_{D2}/C_R and C_f/C_{D1} are independent, that is the error in one ratio does not constitute an error in the other ratio even if C_{D1} equals C_{D2}.

The sensitivities of ω_o and Q with respect to the ratios of interest and the clock period are:

$$S_{q_1}^{\omega_o} = 1/2 \quad , \quad S_{q_2}^{\omega_o} = 1/2 \quad , \quad S_T^{\omega_o} = -1$$

$$S_{q_1}^{Q} = 1/2 \quad , \quad S_{q_2}^{Q} = 1/2 \quad , \quad S_{q_3}^{Q} = 1$$

All of these sensitivities are of the same order as sensitivities for passive element filters. Replacement of the passive inductor in ladder structure filters by the switched-capacitor simulated inductor circuit will have sensitivities equal to a passive filter and generally better than active-RC filters. Since the control of capacitor ratios accuracies is within 1%, the actual errors in ω_o and Q for a circuit using the simulated inductor will be smaller than the errors of passive and active-RC filters because these latter circuits rely on the absolute values of their components.

CHAPTER IV

CIRCUIT SIMULATION

Ideally, the analog reference filter, ARF, of figure 3.6 should be used to simulate the performance of the bilinear inductor once the ARF is realized with switched-capacitor components. Unfortunately, development of the entire bilinear filter from the ARF is the subject of another thesis. Therefore, two simple approaches are used in verifying the circuit's performance. One is the computation of the response of the bilinear z domain equation related to the ARF filter. The other takes advantage of the circuits ability to realize a parallel LC structure.

A bilinear transformation of equation 3.8 can be used to illustrate the need for the proposed bilinear inductor and can also be used to calculate the filter's frequency response. The point at which the mathematical transformation and manipulation of equation 3.8 is most interesting is given below.

$$\frac{V_{out}}{V_{in}} = \frac{C_D(1 - z)}{C_D(1 - z^{-1}) + \frac{T^2}{4L}\frac{(1 + z^{-1})^2}{(1 - z^{-1})} + \frac{T}{2R}(1 + z^{-1})}$$

Note that the bilinear form of the inductor, see equation 2.5, is present in the denominator. A computer computation of the frequency response of this equation was made with ω_o = 10khz, Q = 1/2 and a passband gain of unity, see appendix A pages 45 & 46. The calculated response gave a stopband slope of 40dB/dec, -6dB at ω_o and a gain of unity in the

passband, which is what would be realized with the second-order high-pass

ARF. If ideal bilinear components replace the passive components in the ARF a bilinear, second-order high-pass filter would be created.

The second method for verifying the circuit's operation involves the simulation of a band pass filter. With the addition of two capacitors and four MOS switches, see figure 4.1, the proposed circuit can realize a second-order band pass filter.

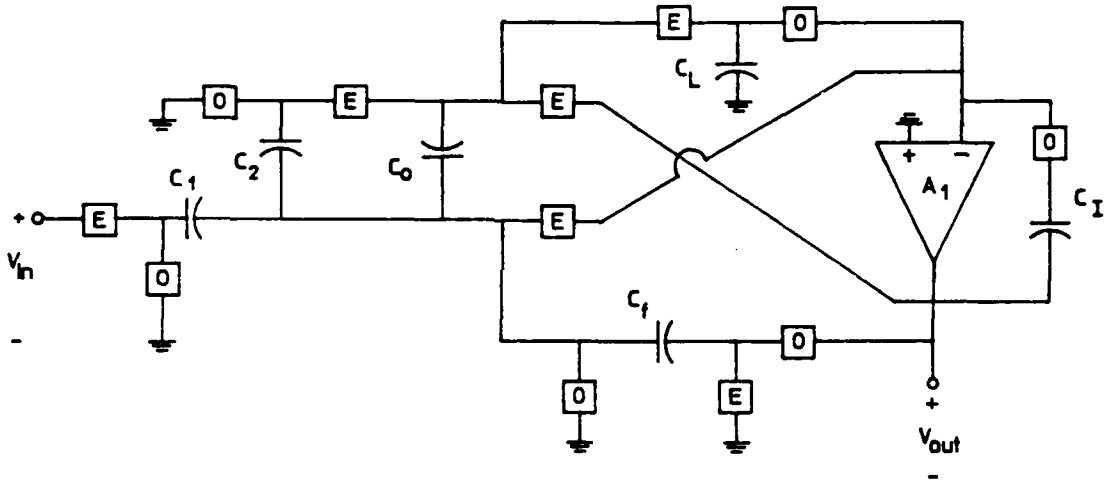

Figure 4.1 Band pass filter.

This method takes advantage of the circuit's ability to simulate a parallel LC structure as well as an inductor. The s-domain transfer function for the filter is

$$\frac{V_{out}}{V_{in}} = \frac{S\ C_1/C_oT}{S^2 + S\ \frac{C_2}{TC_o} + \frac{C_LC_f}{T^2C_IC_o}}$$

From this equation ω_o and the bandwidth, BW, as well as the passband gain, G, can be determined and are

$$\omega_o = \frac{1}{T}\sqrt{\frac{C_L C_f}{C_I C_o}} \quad , \qquad BW = \frac{C_2}{TC_o} \quad , \qquad G = \frac{C_1}{C_2} \quad .$$

The program SWITCAP [14] was used to simulate the circuit of figure 4.1. For simulation purposes a switching frequency of 200khz was used. The center frequency, ω_o, was set at 10khz, bandwidth was set at 1khz and the passband gain set at unity. The frequency response results were excellent, see appendix A pages 47 & 48, with a maximum gain of 1 in the passband and -3dB at 10khz ± 500hz, the performance of the filter and, by implication, the inductor circuit is verified.

CHAPTER V

SUMMARY AND CONCLUSIONS

The focus of this thesis was the synthesis and analysis of a bilinear grounded inductor for use as a direct replacement for the inductance element in a passive ladder filter. The synthesis portion of this thesis consists of the mathematical development of a circuit to replace the passive inductor. The analysis portion includes material on capacitor ratios, parasitics, dynamic range, gain-bandwidth, sensitivity and circuit verification through simulation.

In chapter II, the equations that define the inductor in the s- and z domains were developed. Next, Burton's [4] leap-frog circuit was analyzed and then developed into a LDI type inductor which was finally converted into the bilinear grounded inductor proposed by Inoue & Ueno [8]. This circuit could replace an inductor or a parallel LC structure and was shown to have a large range of possible inductances. A parallel capacitor, C_o, was needed to cancel out a negative capacitance associated with the circuit's bilinear definition. Since C_o was needed to complete the circuit in the first place, it can be used in the cancelation and can be increased to help realize a parallel LC.

Five areas were covered in chapter III on integration limits, nonideal effects and performance. Capacitor ratios, of major importance in switched-capacitor circuits, were analyzed first, and it was shown that capacitors C_I and C_o should be kept as large as practical to minimize process errors. Since C_o is used to cancel a negative capacitance, it is not always possible to make C_o large. It was also concluded that

inductance values would be hard to control due to the inductance's dependance on the absolute value of a capacitor, but regulation was possible by changing the clock frequency. When used in a switched-capacitor filter configuration ω_o is dependent on $L_{eq}C$ which is a function of capacitor ratios, not on the absolute value of L.

Parasitic capacitances are the single most important factor causing distortions in the response of a circuit that is sensitive to stray-capacitances. Capacitor C_o was shown to have no parasitic problems. The inverting capacitor, C_f, will also have no problems if $f_t > 5f_c$; actually this limit is a requirement for switched-capacitor circuits in general. C_I has a problem with leakage current, but for the high switching frequencies normally used, the loss is negligible. C_L does have a problem with top plate parasitics, but they can be partially compensated for by increasing C_L's absolute value.

Dynamic range was shown to be limited by several factors. First, the maximum input voltage was limited by the linear range of the op-amp, which is a function of gain and the power supply voltage. Minimum input voltage levels were limited by the noise levels associated with the op-amp and MOS switches as well as the aliasing of the noise power into the baseband. Given these limits, maximum and minimum input voltages were calculated, and from these results the dynamic range was computed.

Finite gain and bandwidth of op-amps have substantial effects on continuous-time active circuits, but for the proposed circuit and switched-capacitor circuits in general, it was determined that there is little effect from these nonideal op-amp characteristics. The sampling

nature of this circuit allows sufficient settling time between samples to negate the effects of a finite gain-bandwidth.

Finally, a sensitivity study was performed on a second-order bilinear filter that incorporates the proposed circuit. Sensitivities in terms of capacitor ratios were shown to be the same order of magnitude as sensitivities common to passive ladder structures. Given that capacitor ratios can usually be realized with errors of less then 1%, variations in ω_o and Q will be smaller for the switched-capacitor circuit than for a passive circuit which relies on the absolute value of a component whose tolerances are larger than capacitor ratio errors.

Chapter IV dealt with simulation of the bilinear equation defining the ARF filter proposed in the section on sensitivity, and with the simulation of a simple band pass filter to verify that the inductor works. The computer calculation for the ARF filter gave excellent results in terms of modeling a high-pass filter. The band pass filter was designed to give a bandwidth of 1khz at a center frequency of 10khz which it realized. Thus, this circuit can be used as either a bilinear grounded inductor as proposed or as a parallel LC circuit.

RECOMMENDATIONS

Like most theses, this one does not cover all possible areas of interest or all possible solutions to a problem. It may be possible to create or find a circuit that can not only simulate a grounded inductor but does so with fewer components and less sensitivity to parasitic capacitances. In regard to the proposed circuit, there are several areas that require further investigation.

First, nonideal effects associated with the MOS switches were not covered. MOS transistor noise as it effects dynamic range was dealt with, but other aspects like clock feedthrough and the switch construction itself were not. Since these nonideal effects can greatly distort a circuit's response, more work in this area is called for.

While noise sources were considered when the dynamic range was calculated, ways of minimizing the magnitudes of the noise were only mentioned. Noise suppression studies in relation to the proposed circuit and switched-capacitor circuits in general would provided valuable information for future work.

Some limits were stated on what the circuit can achieve in the way of inductances. The full range of possible inductances and cutoff frequencies should be determined in terms of the maximum and minimum range of realizable capacitors.

One last recommendation is to encourage the development of the switched-capacitor version of the analog reference filter. The development would provide insight into the actual construction of switched-capacitor ladder structures.

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APPENDIX A

CIRCUIT SIMULATION

INPUT & OUTPUT

FILES

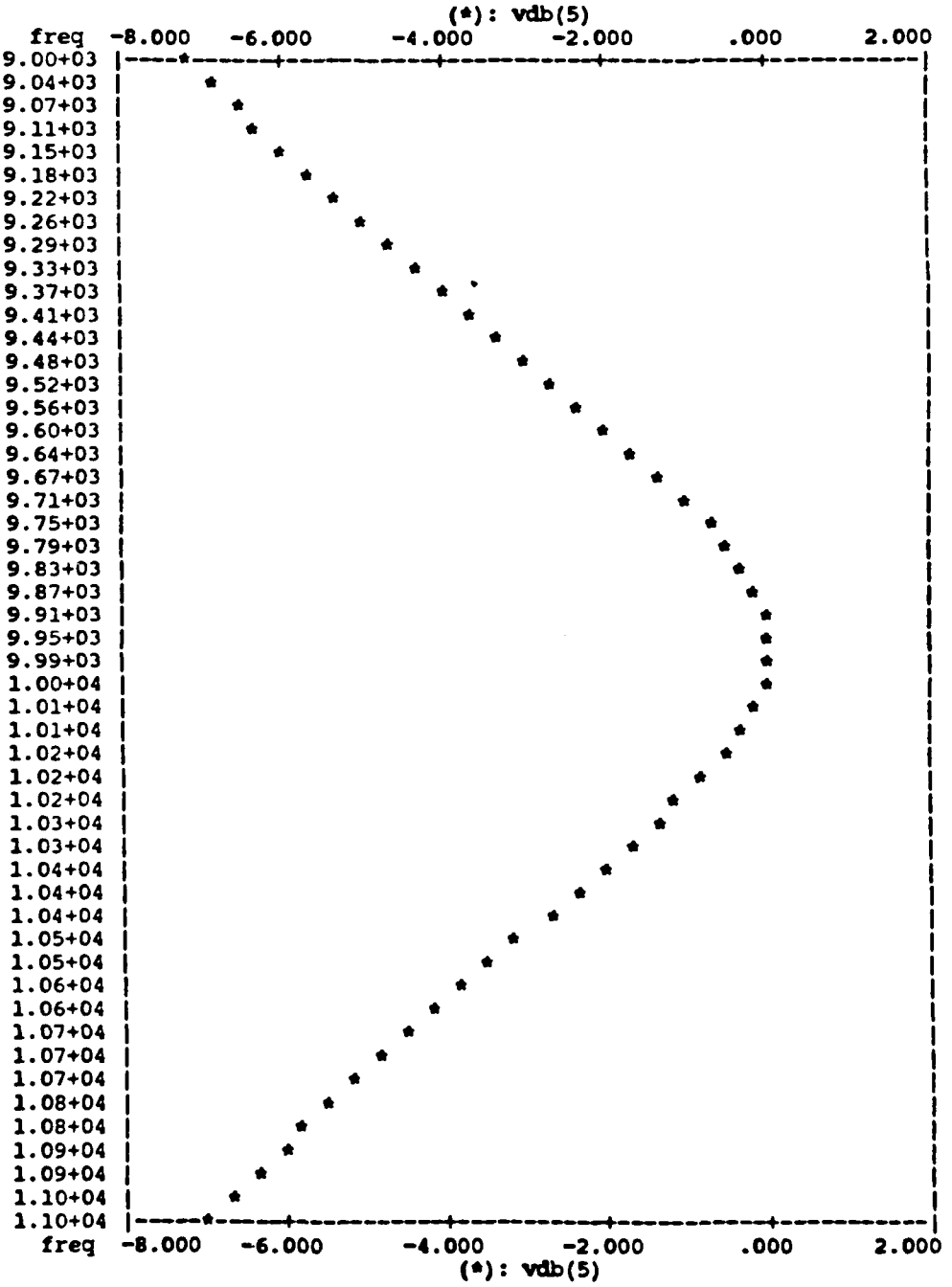
```
C
C$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
C$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
C
C Put the transfer function here
C
      Zinv( Z ) = 1 / Z

      G ( S ) = 0.28

      H ( Z ) = Cd * ( 1 - Zinv( Z ) ) /
     1    (Cd * ( 1 - Zinv( Z )) + Cl*Cf*(1 + Zinv( Z ))*
     1    (1 + Zinv( Z ))/(4*Ci*(1 - Zinv( Z ))) + Cr*(1 + Zinv( Z )))

      Cd = 3.183
      Ci = 3.183
      Cl = 1
      Cf = 1
      Cr = 1
C
C$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
C$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
C
```

Sample frequency is: 200000.0

Frequency	H(Z)-Gain	H(Z)-DB
500.0000	.2493713E-02	-52.06307
562.5000	.3154051E-02	-50.02263
625.0000	.3891059E-02	-48.19864
687.5000	.4704400E-02	-46.54991
750.0000	.5593706E-02	-45.04601
812.5000	.6558571E-02	-43.66382
875.0000	.7598559E-02	-42.38538
937.5000	.8713200E-02	-41.19645
1000.000	.9901994E-02	-40.08555
1125.000	.1249987E-01	-38.06189
1250.000	.1538757E-01	-36.25660
1375.000	.1855997E-01	-34.62845
1500.000	.2201152E-01	-33.14700
1625.000	.2573623E-01	-31.78910
1750.000	.2972772E-01	-30.53677
1875.000	.3397921E-01	-29.37574
2000.000	.3848359E-01	-28.29449
2250.000	.4822097E-01	-26.33528
2500.000	.5887705E-01	-24.60108
2750.000	.7038529E-01	-23.05036
3000.000	.8267637E-01	-21.65237
3250.000	.9567915E-01	-20.38365
3500.000	.1093216	-19.22588
3750.000	.1235314	-18.16445
4000.000	.1382372	-17.18750
4500.000	.1688580	-15.44957
5000.000	.2006498	-13.95123
5500.000	.2331246	-12.64824
6000.000	.2658504	-11.50726
6500.000	.2984560	-10.50239
7000.000	.3306318	-9.61310
7500.000	.3621272	-8.82277
8000.000	.3927463	-8.11775
9000.000	.4508104	-6.92012
10000.00	.5041206	-5.94931
11000.00	.5524567	-5.15403
12000.00	.5959135	-4.49633
13000.00	.6347709	-3.94765
14000.00	.6694043	-3.48623
15000.00	.7002243	-3.09525
16000.00	.7276411	-2.76165
18000.00	.7737878	-2.22756
20000.00	.8105501	-1.82440
22000.00	.8400719	-1.51367
24000.00	.8639975	-1.26975
26000.00	.8835720	-1.07516
28000.00	.8997362	-0.91769
30000.00	.9132034	-0.78864
32000.00	.9245179	-0.68169

```
**************************************************
Input Listing
**************************************************
 TITLE:SIMULATED INDUCTOR BPF -- ROBERT FLYNN

 TIMING;
    PERIOD 5.0E-6;
    CLOCK CLK 1 (0 1/2);
 END;

 CIRCUIT;
    S1   (1 2)   #CLK;
    S2   (2 0)    CLK;
    S3   (4 0)    CLK;
    S4   (4 5)   #CLK;
    S6   (3 0)    CLK;
    S7   (3 8)   #CLK;
    S8   (6 0)   #CLK;
    S9   (6 7)    CLK;
    S10  (5 7)   #CLK;
    S11  (5 10)  #CLK;
    S12  (8 10)   CLK;
    S13  (8 9)    CLK;
    CR1  (2 3)    0.10;
    CR2  (3 4)    0.10;
    CO   (5 3)    3.1831;
    CF   (3 6)    1.00;
    CL   (10 0)   1.00;
    CI   (7 9)    3.1831;
    E1  (7 0 0 8) 5000;
    V1  (1 0);
 END;

 ANALYZE SSS;
    INFREQ 9000 11000 LOG 51;
    SET V1 AC 1.0 0.0;
    SAMPLE OUTPUT HOLD 1 7/8-;
    PLOT VDB(5);
 END;

 END;
```

```
**********************************************************************
SIMULATED INDUCTOR BPF -- ROBERT FLYNN
Sinusoidal Steady State Analysis
**********************************************************************
```




```
*switcap: end of run
```